AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-17 (cancelled)

18. (new) A method of forming an electrical structure on a substrate, the method comprising:

performing a plasma doping (PLAD) operation to form a first doped region in a substrate; and

performing a second doping operation, the second doping operation comprising depositing dopants in the first doped region and in a second doped region that is contiguous with and extends below the first doped region, wherein the first doped region has a higher dopant concentration than the second doped region, the second doped region having a lower periphery that is substantially planar and substantially parallel to the substrate.

19. (new) A method as defined in claim 18, wherein the first doped region has a dopant concentration that terminates relatively abruptly at an uneven lower periphery.

20. (new) A method as defined in claim 18, wherein:

the first doped region has a lower periphery at a depth of less than about 1000 Å; and

the second doped region has a lower periphery at a depth that is less than about 1750 Å and at least about 250 Å greater than the depth of the lower periphery of the first doped region.

21. (new) A method as defined in claim 18, further comprising annealing the substrate after the second doping operation and/or after the PLAD operation to cause a more uniform distribution of dopants than prior to the annealing.

22. (new) A method as defined in claim 21, wherein the annealing is performed as a rapid thermal anneal.

23. (new) A method as defined in claim 18, wherein:

the PLAD operation is conducted at an energy in a range from about 5 KeV to about 15 KeV such that the first doped region has a dopant concentration in a range from about $1x10^{19}$ dopant atoms/cm^3 to about $5x10^{21}$ dopant atoms/cm^3; and

the second doping operation is performed at an energy in a range from about 10 KeV to about 25 KeV such that the second doped region has a dopant concentration in a range from about $1x10^{16}$ dopant atoms/cm^3 to about $1x10^{19}$ dopant atoms/cm^3, the second doping operation being conducted in a medium power implanter operating in a range from about 0 KeV to about 200 KeV.

24. (new) A method as defined in claim 18, wherein the first doped region and the second doped region form a portion of an electrical device that is selected from the group consisting of a diode, a resistor, and a transistor.

25. (new) A method of forming an electrical structure on a substrate, the method comprising:

performing a first doping operation on a substrate, the first doping operation comprising depositing dopants to a first depth within the substrate to form a first doped region, wherein the first doped region has a lower periphery that is substantially planar and substantially parallel to the substrate;

after performing the first doping operation, forming an electrically insulating layer over the substrate; and

performing a plasma doping (PLAD) operation to form a second doped region within the substrate, wherein the second doped region is formed through the electrically insulating layer and wherein the second doped region has a higher dopant concentration than the first doped region, is at least partially circumscribed by the first doped region, and has a shallower lower periphery than the lower periphery of the first doped region.

26. (new) A method as defined in claim 25, wherein the electrically insulating layer comprises tetraethyl orthosilicate.

27. (new) A method as defined in claim 25, wherein the electrically insulating layer has a thickness of from about 50 Å to about 100 Å.

28. (new) A method as defined in claim 25, wherein:

the second depth is less then about 1000 Å; and

the first depth is less than about 1750 Å and at least about 250 Å greater than the second depth.

29. (new) A method as defined in claim 25, further comprising annealing the substrate after the first doping operation and/or after the PLAD operation to cause a more uniform distribution of dopant than prior to the annealing.

30. (new) A method as defined in claim 29, wherein the annealing is performed as a rapid thermal anneal.

31. (new) A method as defined in claim 25, wherein:

the PLAD operation is conducted at an energy in a range from about 5 KeV to about 15 KeV such that the second doped region has a dopant concentration in a range from about 1×10^{19} dopant atoms/cm^3 to about 5×10^{21} dopant atoms/cm^3; and

the first doping operation is performed at an energy in a range from about 10 KeV to about 25 KeV such that the first doped region has a dopant concentration in a range from about 1×10^{16} dopant atoms/cm^3 to about 1×10^{19} dopant atoms/cm^3, the first doping operation being conducted in a medium power implanter operating in a range from about 0 KeV to about 200 KeV.

32. (new) A method as defined in claim 25, wherein the first doped region and the second doped region form a portion of an electrical device that is selected from the group consisting of a diode, a resistor, and a transistor.

33. A method of forming an electrical structure on a substrate, the method comprising:

providing a gate region over a substrate, the gate region having a bottom surface;

performing a plasma doping (PLAD) operation to form a first doped region in a substrate, wherein the first doped region does not underlap the bottom surface of the gate region; and

performing a second doping operation, the second doping operation comprising depositing dopants in the first doped region and in a second doped region that is contiguous with and extends below the first doped region, wherein the first doped region has a higher dopant concentration than the second doped region, the second doped region having at least a portion thereof that underlaps the bottom surface of the gate region.

34. (new) A method as defined in claim 33, wherein the first doped region has a dopant concentration that terminates relatively abruptly at an uneven lower periphery.

35. (new) A method as defined in claim 33, wherein:

the first doped region has a lower periphery at a depth of less then about 1000 Å; and

the second doped region has a lower periphery at a depth that is less than about 1750 Å and at least about 250 Å greater than the depth of the lower periphery of the first doped region.

36. (new) A method as defined in claim 33, further comprising annealing the substrate after the second doping operation and/or after the PLAD operation to cause a more uniform distribution of dopant than prior to the annealing.

37. (new) A method as defined in claim 36, wherein the annealing is performed as a rapid thermal anneal.

38. (new) A method as defined in claim 33, wherein:

the PLAD operation is conducted at an energy in a range from about 5 KeV to about 15 KeV such that the first doped region has a dopant concentration in a range from about 1×10^{19} dopant atoms/cm^3 to about 5×10^{21} dopant atoms/cm^3; and

the second doping operation is performed at an energy in a range from about 10 KeV to about 25 KeV such that the second doped region has a dopant concentration in a range from about 1×10^{16} dopant atoms/cm^3 to about 1×10^{19} dopant atoms/cm^3, the second doping operation being conducted in a medium power implanter operating in a range from about 0 KeV to about 200 KeV.

39. (new) A method as defined in claim 33, wherein the first doped region and the second doped region form a portion of an electrical device that is selected from the group consisting of a diode, a resistor, and a transistor.

40. (new) A method of forming an electrical structure on a substrate, the method comprising:

providing a gate region over a substrate, the gate region having a bottom surface;

performing a first doping operation on the substrate, the first doping operation comprising depositing dopants to a first depth within the substrate to form a first doped region, wherein the first doped region has at least a portion thereof that underlaps the bottom surface of the gate region;

after performing the first doping operation, forming an electrically insulating layer over the substrate; and

performing a plasma doping (PLAD) operation on the substrate, the PLAD operation comprising depositing dopants to a second depth within the substrate to form a second doped region within the substrate, wherein the second depth is less than the first depth and wherein the second doped region is formed through the electrically insulating layer, has a higher dopant concentration than the first doped region, is at least partially circumscribed by the first doped region, and does not underlap the bottom surface of the gate region.

41. (new) A method as defined in claim 40, wherein the electrically insulating layer comprises tetraethyl orthosilicate.

42. (new) A method as defined in claim 41, wherein the electrically insulating layer has a thickness of from about 50 Å to about 100 Å.

43. (new) A method as defined in claim 40, wherein:

the second depth is less then about 1000 Å; and

the first depth is less than about 1750 Å and at least about 250 Å greater than the second depth.

44. (new) A method as defined in claim 40, further comprising annealing the substrate after the first doping operation and/or after the PLAD operation to cause a more uniform distribution of dopant than prior to the annealing.

45. (new) A method as defined in claim 44, wherein the annealing is performed as a rapid thermal anneal.

46. (new) A method as defined in claim 40, wherein:

the PLAD operation is conducted at an energy in a range from about 5 KeV to about 15 KeV such that the second doped region has a dopant concentration in a range from about $1x10^{19}$ dopant atoms/cm^3 to about $5x10^{21}$ dopant atoms/cm^3; and

the first doping operation is performed at an energy in a range from about 10 KeV to about 25 KeV such that the first doped region has a concentration in a range from about $1x10^{16}$ dopant atoms/cm^3 to about $1x10^{19}$ dopant atoms/cm^3, the first doping operation being conducted in a medium power implanter operating in a range from about 0 KeV to about 200 KeV.

47. (new) A method as defined in claim 40, wherein the first doped region and the second doped region form a portion of an electrical device that is selected from the group consisting of a diode, a resistor, and a transistor.